Chapter 2 – c2000 Processor Hardware

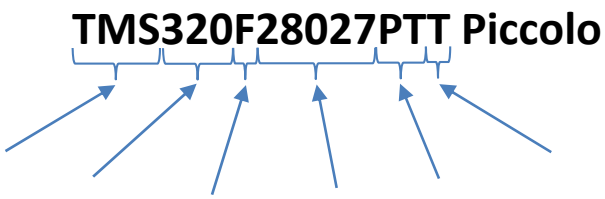
Introduction

The c2000 family has a number of processors to choose from. They differ in one or more of the following areas:

- package
- program memory size (Flash)
- data memory size (RAM)
- with or without floating-point unit
- maximum clock rate
- cost

The basic architecture and underlying assembly language of the processor is similar amongst all the parts.

The part that we are using on the LaunchPad is:



The c2000 family has been around since 1995 when it was a 16-bit processor. The Piccolo is a fixed-point 32-bit processor that was introduced in 2009 and continues to be an active product with dozens of variations to choose from. It combines the flexibility and stand-alone features of a microcontroller with the fast processing speed of a DSP which makes it a good candidate for embedded real-time applications.

The following information is relevant to the TMS320F28027PTT chip unless otherwise noted.

Cost

CAN$5.49 ea (in 1000 lot)

CAN$9.69 (in single lot from DigiKey)

Package

48-pin LQFP

Junction Width

90 nm (originally) *(should be smaller now)*

Power

One single 3.3V supply:

no power sequencing required

Power Consumption: +3.3 V @ 118 mA or less = 0.4 W or less

(note: internal core = 1.8 V)

I/O Levels: TTL-compatible CMOS levels

Operating Temperature Range

−40 to +105 °C (at junction)

On-Chip Peripherals include:

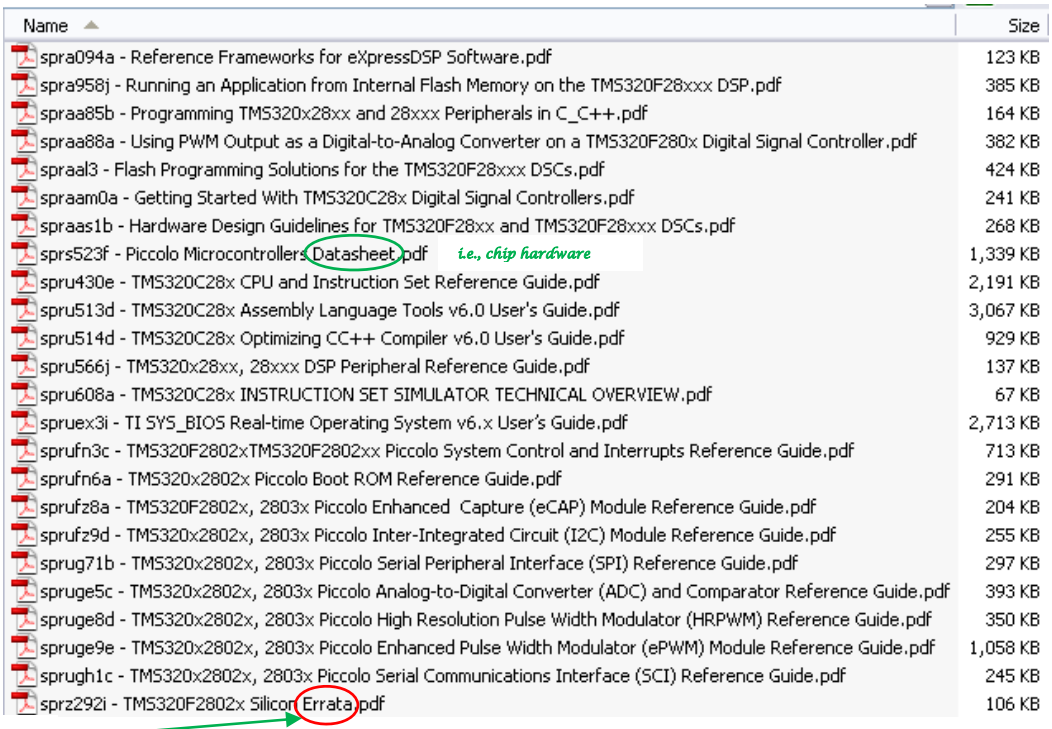
- serial communication buses:
  - SPI (one) ← *synchronous (clock, frame, data in, data out), e.g.*
  - SCI (one) ← *asynchronous (data in, data out), e.g.*
  - I^2C (one) ← *synchronous (clock (2-way), data (2-way), e.g.*

- A-D Converter:
  - up to 13 input channels multiplexed onto two sample-and-hold buffers onto one 12-bit converter
  - up to 4.6 Msamples/sec

- PWM outputs *e.g.* *e.g.*

- GPIO:
  - up to 22 lines available
  - "qualified" re. metastability

Documentation



Name	Size
spra094a - Reference Frameworks for eXpressDSP Software.pdf	123 KB
spra958j - Running an Application from Internal Flash Memory on the TMS320F28xxx DSP.pdf	385 KB
spraa85b - Programming TMS320x28xx and 28xxx Peripherals in C_C++.pdf	164 KB
spraa88a - Using PWM Output as a Digital-to-Analog Converter on a TMS320F280x Digital Signal Controller.pdf	382 KB
spraal3 - Flash Programming Solutions for the TMS320F28xxx DSCs.pdf	424 KB
spraam0a - Getting Started With TMS320C28x Digital Signal Controllers.pdf	241 KB
spraas1b - Hardware Design Guidelines for TMS320F28xx and TMS320F28xxx DSCs.pdf	268 KB
sprs523f - Piccolo Microcontrollers Datasheet.pdf *i.e., chip hardware*	1,339 KB
spru430e - TMS320C28x CPU and Instruction Set Reference Guide.pdf	2,191 KB
spru513d - TMS320C28x Assembly Language Tools v6.0 User's Guide.pdf	3,067 KB
spru514d - TMS320C28x Optimizing CC++ Compiler v6.0 User's Guide.pdf	929 KB
spru566j - TMS320x28xx, 28xxx DSP Peripheral Reference Guide.pdf	137 KB
spru608a - TMS320C28x INSTRUCTION SET SIMULATOR TECHNICAL OVERVIEW.pdf	67 KB
spruex3i - TI SYS_BIOS Real-time Operating System v6.x User's Guide.pdf	2,713 KB
sprufn3c - TMS320F2802xTMS320F2802xx Piccolo System Control and Interrupts Reference Guide.pdf	713 KB
sprufn6a - TMS320x2802x Piccolo Boot ROM Reference Guide.pdf	291 KB
sprufz8a - TMS320F2802x, 2803x Piccolo Enhanced Capture (eCAP) Module Reference Guide.pdf	204 KB
sprufz9d - TMS320x2802x, 2803x Piccolo Inter-Integrated Circuit (I2C) Module Reference Guide.pdf	255 KB
sprug71b - TMS320x2802x, 2803x Piccolo Serial Peripheral Interface (SPI) Reference Guide.pdf	297 KB
spruge5c - TMS320x2802x, 2803x Piccolo Analog-to-Digital Converter (ADC) and Comparator Reference Guide.pdf	393 KB
spruge8d - TMS320x2802x, 2803x Piccolo High Resolution Pulse Width Modulator (HRPWM) Reference Guide.pdf	350 KB
spruge9e - TMS320x2802x, 2803x Piccolo Enhanced Pulse Width Modulator (ePWM) Module Reference Guide.pdf	1,058 KB
sprugh1c - TMS320x2802x, 2803x Piccolo Serial Communications Interface (SCI) Reference Guide.pdf	245 KB
sprz292i - TMS320F2802x Silicon Errata.pdf	106 KB

designer: keep up-to-date on these! (sign up for "Alerts")

Total number of pages of documentation listed above = ?

Datasheet – 138 pages

TMS320F28027, TMS320F28026, TMS320F28023, TMS320F28022
TMS320F28021, TMS320F28020, TMS320F280200

SPRS523K – NOVEMBER 2008 – REVISED JUNE 2016

TMS320F2802x Piccolo™ Microcontrollers

1 Device Overview

1.1 Features

- High-Efficiency 32-Bit CPU (TMS320C28x)
  - 60 MHz (16.67-ns Cycle Time)
  - 50 MHz (20-ns Cycle Time)
  - 40 MHz (25-ns Cycle Time)
  - 16 × 16 and 32 × 32 MAC Operations
  - 16 × 16 Dual MAC
  - Harvard Bus Architecture
  - Atomic Operations
  - Fast Interrupt Response and Processing
  - Unified Memory Programming Model
  - Code-Efficient (in C/C++ and Assembly)
- Endianness: Little Endian
- Low Cost for Both Device and System:
  - Single 3.3-V Supply
  - No Power Sequencing Requirement
  - Integrated Power-on and Brown-out Resets
  - Small Packaging, as Low as 38-Pin Available
  - Low Power
  - No Analog Support Pins
- Clocking:
  - Two Internal Zero-Pin Oscillators
  - On-Chip Crystal Oscillator and External Clock Input
  - Watchdog Timer Module
  - Missing Clock Detection Circuitry
- Up to 22 Individually Programmable, Multiplexed GPIO Pins With Input Filtering
- Peripheral Interrupt Expansion (PIE) Block That Supports All Peripheral Interrupts
- Three 32-Bit CPU Timers
- Independent 16-Bit Timer in Each Enhanced Pulse Width Modulator (ePWM)
- On-Chip Memory
  - Flash, SARAM, OTP, Boot ROM Available
- Code-Security Module
- 128-Bit Security Key and Lock
  - Protects Secure Memory Blocks
  - Prevents Firmware Reverse Engineering
- Serial Port Peripherals
  - One Serial Communications Interface (SCI) Universal Asynchronous Receiver/Transmitter (UART) Module
  - One Serial Peripheral Interface (SPI) Module
  - One Inter-Integrated-Circuit (I2C) Module
- Enhanced Control Peripherals
  - ePWM
  - High-Resolution PWM (HRPWM)
  - Enhanced Capture (eCAP) Module
  - Analog-to-Digital Converter (ADC)
  - On-Chip Temperature Sensor
  - Comparator
- Advanced Emulation Features
  - Analysis and Breakpoint Functions
  - Real-Time Debug Through Hardware
- 2802x, 2802xx Packages
  - 38-Pin DA Thin Shrink Small-Outline Package (TSSOP)
  - 48-Pin PT Low-Profile Quad Flatpack (LQFP)

1.2 Applications

- White Goods
- Switch Mode Power Supplies (SMPSs)
- DC-DC Multiple-Output Power Supplies
- Solar Micro Inverters and Converters
- LED Lighting
- Power Factor Correction
- Sewing and Textile Machines
- eBikes

Pin-Out - *This sheet used by schematic designer*

2.1 Pin Assignments

Figure 2-1 shows the 48-pin PT plastic quad flatpack (PQFP) pin assignments. Figure 2-2 shows the 38-pin DA plastic small outline package (PSOP) pin assignments.

"bird's eye view"

note: sharing of some pins

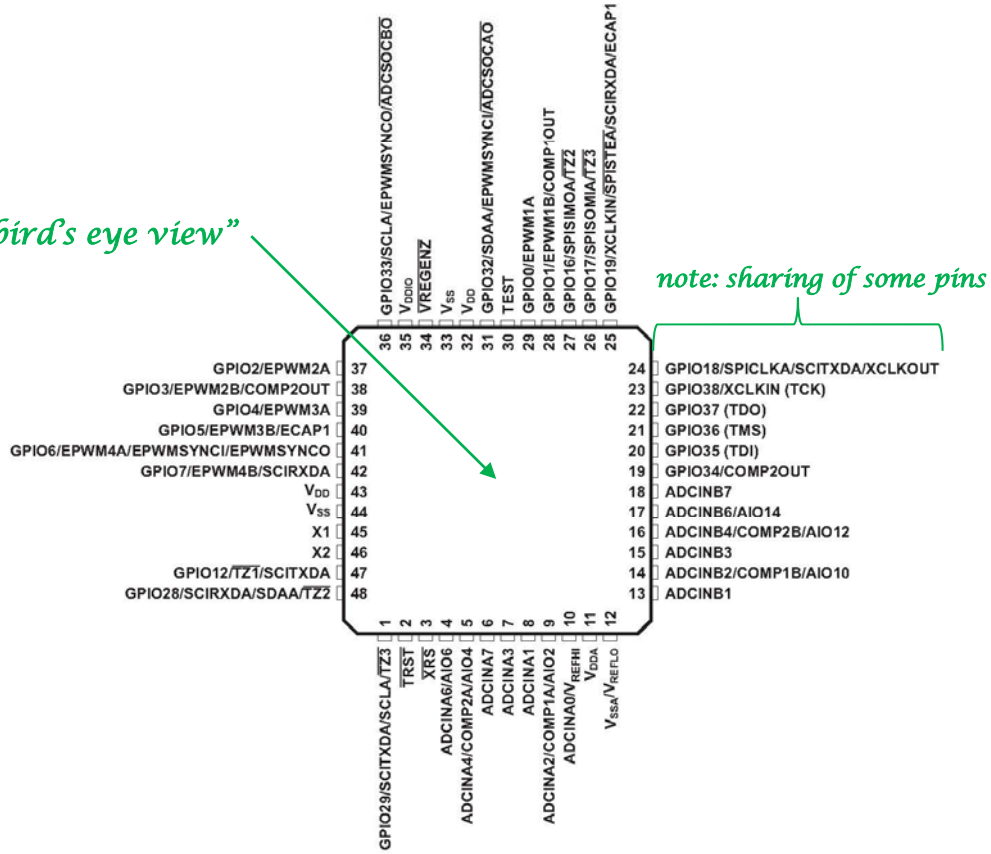


Figure 2-1. 2802x 48-Pin PT PQFP (Top View)

pin sharing:

- *reduces pin count → reduces cost, increases solder joint reliability*
- *but cannot use all functions at same time*

Mechanical - *This sheet used by PCB layout designer*

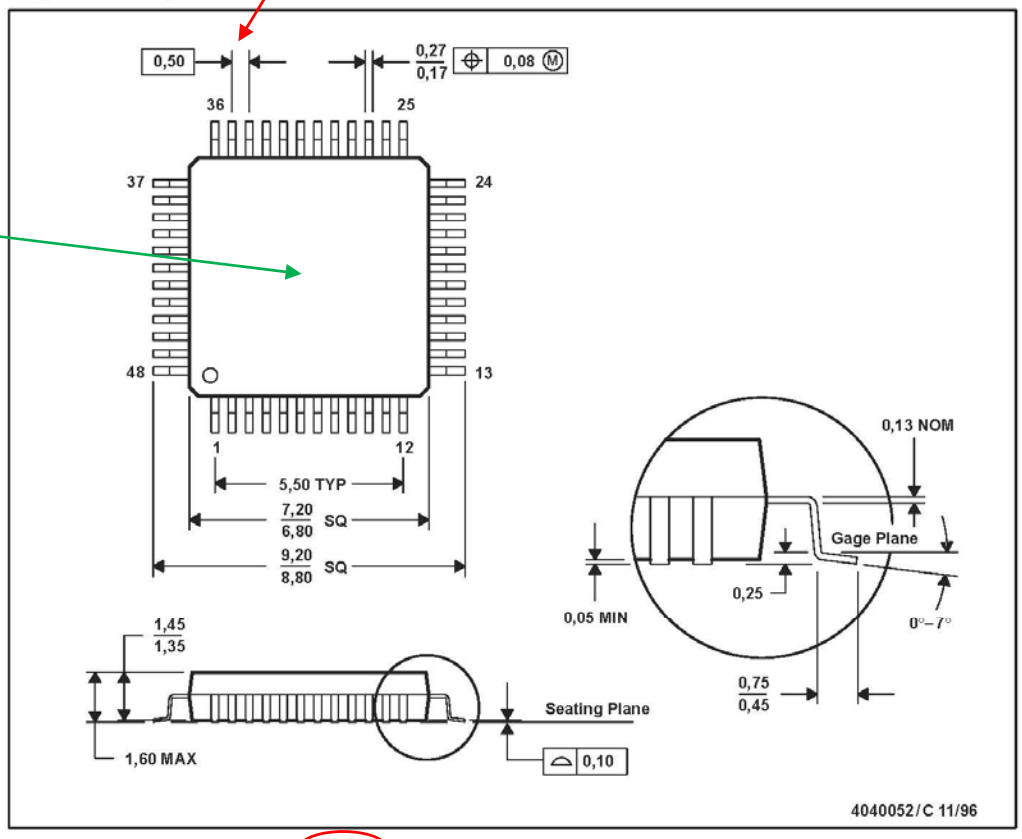
MECHANICAL DATA

"pitch"

MTQF003A – OCTOBER 1994 – REVISED DECEMBER 1996

PT (S-PQFP-G48) **PLASTIC QUAD FLATPACK**

"bird's eye view"



NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS-026
D. This may also be a thermally enhanced plastic package with leads conected to the die pads.

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1

Absolute vs Operating Conditions

TMS320F28027, TMS320F28026, TMS320F28023, TMS320F28022
TMS320F28021, TMS320F28020, TMS320F280200

SPRS523F–NOVEMBER 2008–REVISED DECEMBER 2010 www.ti.com

6 Electrical Specifications

6.1 Absolute Maximum Ratings(1) (2)

Supply voltage range, V_{DDIO} (I/O and Flash)	with respect to V_{SS}	–0.3 V to 4.6 V
Supply voltage range, V_{DD}	with respect to V_{SS}	–0.3 V to 2.5 V
Analog voltage range, V_{DDA}	with respect to V_{SSA}	–0.3 V to 4.6 V
Input voltage range, V_{IN} (3.3 V)		–0.3 V to 4.6 V
Output voltage range, V_O		–0.3 V to 4.6 V
Input clamp current, I_{IK} (V_{IN} < 0 or V_{IN} > V_{DDIO})(3)		±20 mA
Output clamp current, I_{OK} (V_O < 0 or V_O > V_{DDIO})		±20 mA
Junction temperature range, T_J (4)		–40°C to 150°C
Storage temperature range, T_{stg} (4)		–65°C to 150°C

(1) Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under Section 6.2 is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltage values are with respect to V_{SS}, unless otherwise noted.
(3) Continuous clamp current per pin is ± 2 mA.
(4) Long-term high-temperature storage and/or extended use at maximum temperature conditions may result in a reduction of overall device life. For additional information, see *IC Package Thermal Metrics Application Report* (literature number SPRA953) and *Reliability Data for TMS320LF24xx and TMS320F28xx Devices Application Report* (literature number SPRA963).

6.2 Recommended Operating Conditions

		MIN	NOM	MAX	UNIT
Device supply voltage, I/O, V_{DDIO} (1)(2)		2.97	3.3	3.63	V
Device supply voltage CPU, V_{DD} (When internal VREG is disabled and 1.8 V is supplied externally)		1.71	1.8	1.995	V
Supply ground, V_{SS}			0		V
Analog supply voltage, V_{DDA} (1)		2.97	3.3	3.63	V
Analog ground, V_{SSA}			0		V
Device clock frequency (system clock)	28020, 28021, 280200	2		40	MHz
	28022, 28023	2		50	
	28026, 28027	2		60	
High-level input voltage, V_{IH} (3.3 V)		2		V_{DDIO} + 0.3	V
Low-level input voltage, V_{IL} (3.3 V)		V_{SS} – 0.3		0.8	V
High-level output source current, V_{OH} = $V_{OH(MIN)}$, I_{OH}	All GPIO/AIO pins		–4		mA
	Group 2 (3)		–8		mA
Low-level output sink current, V_{OL} = $V_{OL(MAX)}$, I_{OL}	All GPIO/AIO pins		4		mA
	Group 2 (3)		8		mA
Junction temperature, T_J (4)	T version	–40		105	°C
	S version	–40		125	
	Q version (Q100 Qualification)	–40		125	

(1) V_{DDIO} and V_{DDA} should be maintained within ~0.3 V of each other.
(2) A tolerance of ±10% may be used for V_{DDIO} if the BOR is not used. See the *TMS320F28027, TMS320F28026, TMS320F28023, TMS320F28022, TMS320F28021, TMS320F28020, TMS320F280200 Piccolo MCU Silicon Errata* (literature number SPRZ292) for more information. V_{DDIO} tolerance is ±5% if the BOR is enabled.
(3) Group 2 pins are as follows: GPIO16, GPIO17, GPIO18, GPIO19, GPIO28, GPIO29, GPIO36, GPIO37
(4) T_A (Ambient temperature) is product- and application-dependent and can go up to the specified T_J max of the device. See Section 6.5, Thermal Design Considerations.

Why not 0?

re. I/O

6.3 Electrical Characteristics(1)

over recommended operating conditions (unless otherwise noted)

PARAMETER			TEST CONDITIONS		MIN	TYP	MAX	UNIT
V_{OH}	High-level output voltage		I_{OH} = I_{OH} MAX		2.4			V
			I_{OH} = 50 µA		V_{DDIO} – 0.2			
V_{OL}	Low-level output voltage		I_{OL} = I_{OL} MAX				0.4	V
I_{IL}	Input current (low level)	Pin with pullup enabled	V_{DDIO} = 3.3 V, V_{IN} = 0 V	All GPIO/AIO	–80	–140	–205	µA
				$\overline{XRS}$ pin	–225	–290	–360	
		Pin with pulldown enabled	V_{DDIO} = 3.3 V, V_{IN} = 0 V				±2	
I_{IH}	Input current (high level)	Pin with pullup enabled	V_{DDIO} = 3.3 V, V_{IN} = V_{DDIO}				±2	µA
		Pin with pulldown enabled	V_{DDIO} = 3.3 V, V_{IN} = V_{DDIO}		28	50	80	
I_{OZ}	Output current, pullup or pulldown disabled		V_O = V_{DDIO} or 0 V				±2	µA
C_i	Input capacitance					2		pF
	V_{DDIO} BOR trip point		Falling V_{DDIO}		2.42	2.65	3.135	V
	V_{DDIO} BOR hysteresis					35		mV
	Supervisor reset release delay time		Time after BOR/POR/OVR event is removed to $\overline{XRS}$ release		400		800	µs
	VREG V_{DD} output		Internal VREG on			1.9		V

(1) When the on-chip VREG is used, its output is monitored by the POR/BOR circuit, which will reset the device should the core voltage (V_{DD}) go out of range.

also re. I/O

Low-Power Modes – Current Consumption

Table 6-3. TMS320F2802x Current Consumption at 60-MHz SYSCLKOUT

MODE	TEST CONDITIONS	VREG ENABLED				VREG DISABLED					
		I_{DDIO} (1)		I_{DDA} (2)		I_{DD}		I_{DDIO} (1)		I_{DDA} (2)	
		TYP (3)	MAX	TYP (3)	MAX	TYP (3)	MAX	TYP (3)	MAX	TYP (3)	MAX
Operational (Flash)	The following peripheral clocks are enabled: • ePWM1/2/3/4 • eCAP1 • SCI-A • SPI-A • ADC • I2C • COMP1/2 • CPU-TIMER0/1/2 All PWM pins are toggled at 60 kHz. All I/O pins are left unconnected. (4) Code is running out of flash with 2 wait-states. XCLKOUT is turned off.	90 mA	100 mA	13 mA	18 mA	80 mA	90 mA	15 mA	18 mA	13 mA	18 mA
IDLE	Flash is powered down. XCLKOUT is turned off. All peripheral clocks are turned off.	18 mA	23 mA	75 µA	80 µA	19 mA	24 mA	120 µA	400 µA	75 µA	80 µA
STANDBY	Flash is powered down. Peripheral clocks are off.	4 mA	7 mA	10 µA	15 µA	4 mA	7 mA	120 µA	400 µA	10 µA	15 µA
HALT	Flash is powered down. Peripheral clocks are off. Input clock is disabled. (5)	50 µA		10 µA	15 µA	15 µA		25 µA		10 µA	15 µA

(1) I_{DDIO} current is dependent on the electrical loading on the I/O pins.
(2) In order to realize the I_{DDA} currents shown for IDLE, STANDBY, and HALT, clock to the ADC module must be turned off explicitly by writing to the PCLKCR0 register.
(3) The TYP numbers are applicable over room temperature and nominal voltage.
(4) The following is done in a loop:
- Data is continuously transmitted out of SPI-A and SCI-A ports.
- The hardware multiplier is exercised.
- Watchdog is reset.
- ADC is performing continuous conversion.
- COMP1/2 are continuously switching voltages.
- GPIO17 is toggled.

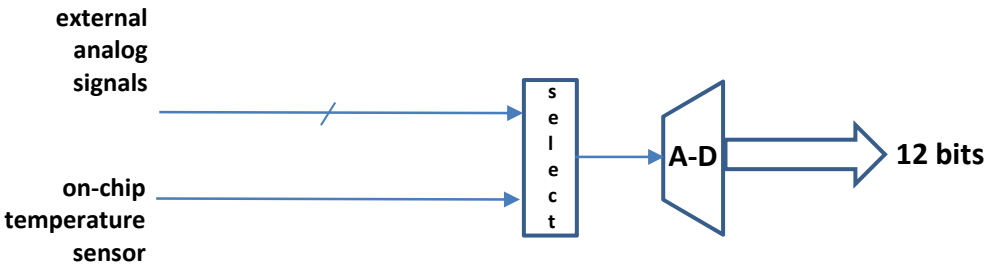
(5) If a quartz crystal or ceramic resonator is used as the clock source, the HALT mode shuts down the on-chip crystal oscillator.

NOTE

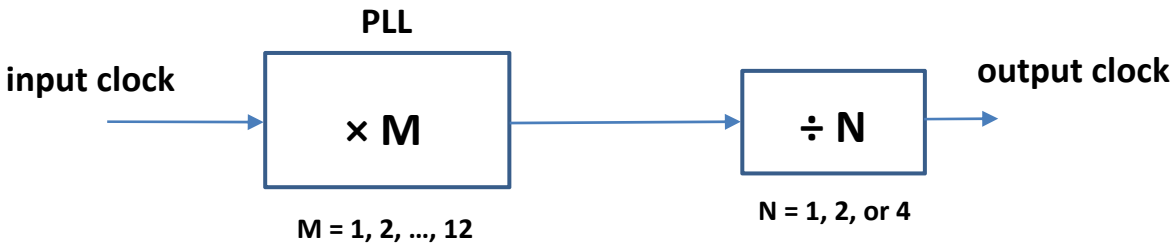
The peripheral - I/O multiplexing implemented in the device prevents all available peripherals from being used at the same time. This is because more than one peripheral function may share an I/O pin. It is, however, possible to turn on the clocks to all the peripherals at the same time, although such a configuration is not useful. If this is done, the current drawn by the device will be more than the numbers specified in the current consumption tables.

More Features:

- temperature sensor – the on-chip temperature can be read via the on-chip A-D



- PLL – generates high-frequency processor clock derived from low-frequency input clock
  - reduces EMI emanating from board
  - allows smooth (no glitch) "on-the-fly" change in processor clock frequency
    - useful for low-power modes



$f_{out} = M \bullet f_{in}$

Default LaunchPad numbers:

Output clock = (input clock = 10 MHz) x (M = 12) ÷ (N = 2) = 60 MHz

- watch-dog (WD) – continuously running counter that resets whenever the key sequence 0x55, 0xAA is written to it; if WD counter overflows, it forces a processor reset

- missing clock detect circuitry – detects when processor clock fails; if so, forces PLL to generate a slow "limping" clock (specified in the range 1 – 5 MHz)

- code security module (CSM) – intended to prevent reverse engineering of user code

Protected Registers

Most registers are write-protected, such as:

- Watch-dog set-up registers
- A-D set-up registers
- Port set-up registers
- etc

This increases the reliability of the system in that it is more difficult for a bug in the code to inadvertently write to a critical register which could mess up things.

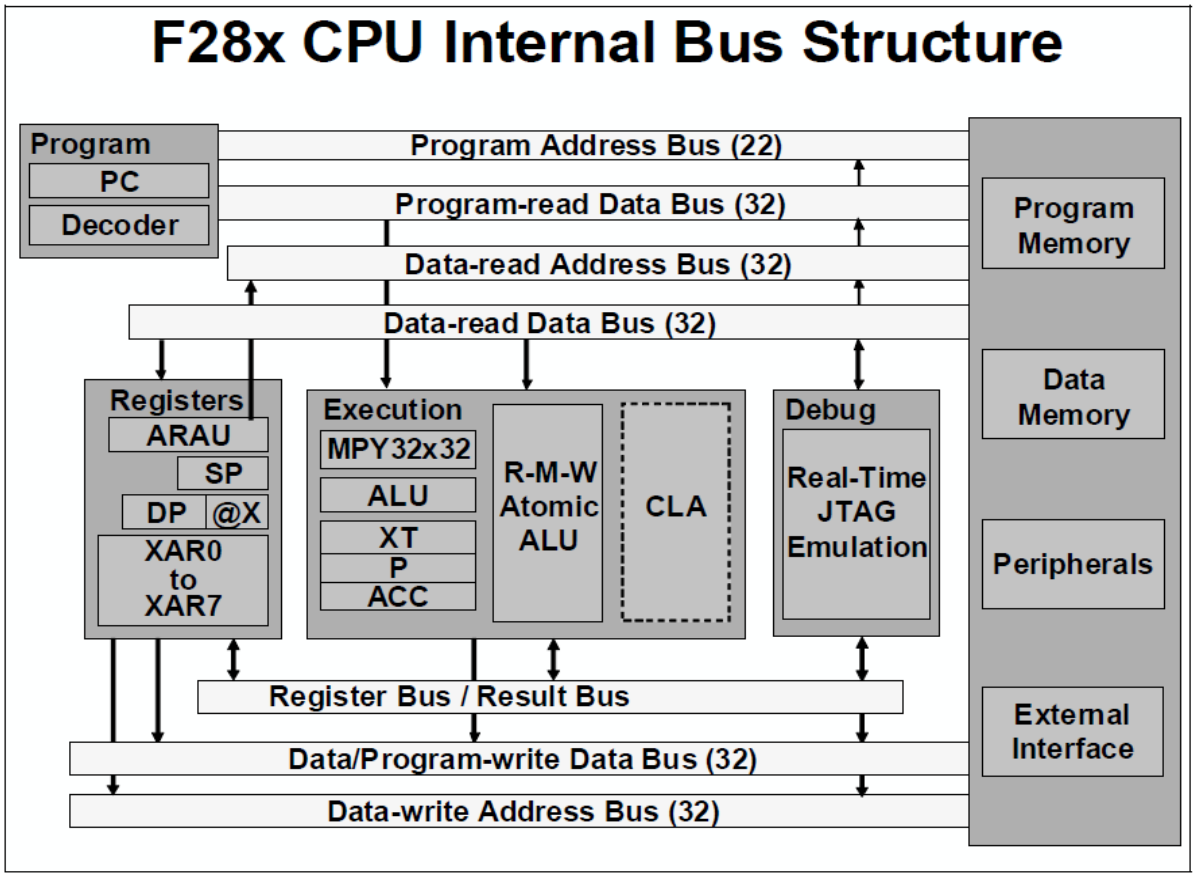
To gain temporary access to registers, e.g. during initialization of the application, the user code can invoke "allow" and disallow instructions:

```
. . .
Allow
Modify register
Disallow
. . .
```

CPU

- 32-bit fixed-point unit
- 32-bit buses
- can do a 32x32 multiply-accumulate operation in one or two cycles
- 8-stage "protected" pipeline
- instruction set includes some "atomic" instructions

useful for multi-tasking
e.g. "test bit and clear" to coordinate sharing of resource between tasks



Memory

- locations contain 16-bit words
  - program instructions can be one or two words in length
  - data can be one or two words in length

  (two words can flow on the 32-bit bus at the same time)

- program address bus = 22 bits → potential for up to 4M addressable program words

- data address bus = 32 bits → potential for up to 4G addressable data words ← 22 used in Piccolo

- Flash: 32Kx16 ← program this for Release

- RAM
  - M0: 1Kx16
  - M1: 1Kx16
  - L0: 4Kx16

- Boot ROM: 8Kx16

- One-Time Programmable(OTP): 1Kx16
  - can contain user's custom bootloader (for special cases)